WHAT IS CLAIMED IS:

1. For use in an integrated circuit of the type comprising at least two power supply domains in which each power supply domain comprises at least one module powered by the same voltage level, an apparatus for blocking an output signal in a first power supply domain from being sent to a second power supply domain when said second power supply domain is in a low power mode.

2. The apparatus as claimed in Claim 1 wherein said apparatus comprises:

a power sense cell within said integrated circuit, said power sense cell capable of determining whether said second power supply domain is in a low power mode, and

a logic circuit capable of blocking said output signal in said first power supply domain from being sent to said second power supply domain when said power sense cell determines that said second power supply domain is in a low power mode.

3. The apparatus as claimed in Claim 2 wherein said logic circuit comprises an AND gate having as a first input said output signal of said first power supply domain, and having as a second input a signal from said power sense cell.

4. The apparatus as claimed in Claim 2 wherein said power sense cell is located within said first power supply domain.

5. The apparatus as claimed in Claim 2 wherein said power sense cell comprises a Schmitt trigger circuit.

6. The apparatus as claimed in Claim 2 further comprising an apparatus for synchronizing blocked clock signals to prevent clock signals from being shortened by a signal from said power sense cell.

7. The apparatus as claimed in Claim 6 wherein said apparatus comprises:

a first D flip flop circuit having as one input a signal from said power sense cell, and having as a second input a clock signal;

a second D flip flop circuit having as one input an output signal from said first D flip flop circuit, and having as a second input said clock signal; and

an AND gate having as one input an output signal from said second D flip flop circuit, and having as a second input said clock signal.

8. For use in an integrated circuit of the type comprising at least two power supply domains in which each power supply domain comprises at least one module powered by the same voltage level, an apparatus for blocking an output signal in a first power supply domain from being received in a second power supply domain when said first power supply domain is in a low power mode.

9. The apparatus as claimed in Claim 8 wherein said apparatus comprises:

a power sense cell within said integrated circuit, said power sense cell capable of determining whether said first power supply domain is in a low power mode, and

a logic circuit capable of blocking said output signal from said first power supply domain from being received in said second power supply domain when said power sense cell determines that said first power supply domain is in a low power mode.

10. The apparatus as claimed in Claim 9 wherein said logic circuit comprises an AND gate having as a first input said output signal from said first power supply domain, and having as a second input a signal from said power sense cell.

11. The apparatus as claimed in Claim 9 wherein said power sense cell is located within said second power supply domain.

12. The apparatus as claimed in Claim 9 wherein said power sense cell comprises a Schmitt trigger circuit.

13. The apparatus as claimed in Claim 9 further comprising an apparatus for synchronizing blocked clock signals to prevent clock signals from being shortened by a signal from said power sense cell.

14. The apparatus as claimed in Claim 13 wherein said apparatus comprises:

a first D flip flop circuit having as one input a signal from said power sense cell, and having as a second input a clock signal;

a second D flip flop circuit having as one input an output signal from said first D flip flop circuit, and having as a second input said clock signal; and

an AND gate having as one input an output signal from said second D flip flop circuit, and having as a second input said clock signal.

15. For use in an integrated circuit of the type comprising at least two power supply domains in which each power supply domain comprises at least one module powered by the same voltage level, a method for blocking an output signal in a first power supply domain from being sent to a second power supply domain when said second power supply domain is in a low power mode, said method comprising the steps of:

sensing with a power sense cell when said second power supply domain is in a low power mode; and

blocking said output signal in said first power supply domain from being sent to said second power supply domain when said power sense cell determines that said second power supply domain is in a low power mode.

16. The method as claimed in Claim 15 wherein the step of blocking said output signal in said first power supply domain from being sent to said second power supply domain comprises the steps of:

sending said output signal in said first power supply domain to a first input of an AND gate; and

sending a signal from said power sense cell to a second input of said AND gate.

17. The method as claimed in Claim 15 wherein said power sense cell is located in within said first power supply domain.

18. The method as claimed in Claim 15 wherein said power sense cell comprises a Schmitt trigger circuit.

19. The method as claimed in Claim 15 further comprising the step of:

synchronizing blocked clock signals to prevent clock signals from being shortened by a signal from said power sense cell.

20. For use in an integrated circuit of the type comprising at least two power supply domains in which each power supply domain comprises at least one module powered by the same voltage level, a method for blocking an output signal in a first power supply domain from being received in a second power supply domain when said first power supply domain is in a low power mode, said method comprising the steps of:

sensing with a power sense cell when said first power supply domain is in a low power mode; and

blocking said output signal in said first power supply domain from being received in said second power supply domain when said power sense cell determines that said first power supply domain is in a low power mode.

21. The method as claimed in Claim 20 wherein the step of blocking said output signal in said first power supply domain from being received in said second power supply domain comprises the steps of:

sending said output signal from said first power supply domain to a first input of an AND gate; and

sending a signal from said power sense cell to a second input of said AND gate.

22. The method as claimed in Claim 20 wherein said power sense cell is located in within said second power supply domain.

23. The method as claimed in Claim 20 wherein said power sense cell comprises a Schmitt trigger circuit.

24. The method as claimed in Claim 20 further comprising the step of:

synchronizing blocked clock signals to prevent clock signals from being shortened by a signal from said power sense cell.